AMENDMENTS TO THE CLAIMS

Claims 1–3. (Cancelled)

4. (Currently Amended) A device as claimed in claim 24~~-26~~, wherein the operand mapping unit comprises;

a first multiplexer for providing one of the present luminance signal and the previous luminance signal as a first value 'a' to the numerator generating unit, and

a second multiplexer for providing one of the present luminance signal and the previous luminance signal as a second value 'b' to the numerator generating unit.

5. (Previously Presented) A device as claimed in claim 4, wherein the numerator generating unit comprises:

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the first value >a=, which are first intermediate operands,

a second shift left for shifting the second value >b= from the second multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the second value >b=, which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining final operands and the numerator portion in the conversion equation from the first intermediate operands and the second intermediate operands.

6. (Previously Presented) A device as claimed in claim 5, wherein the operation processing unit comprises:

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the controller,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the controller,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the controller,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

an operator for selectively subjecting a value from the third multiplexer and a value from the fourth multiplexer to a different operation,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator portion f1 of the conversion equation.

7. (Original) A device as claimed in claim 6, wherein the operator is either an adder or a subtracter.

8. (Previously Presented) A device as claimed in claim 24, wherein the denominator generating unit comprises:

a shift right shifting the numerator portion f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values 2, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator portion of the conversion equation and a luminance signal having a final converted format using the plurality of values.

9. (Previously Presented) A device as claimed in claim 8, wherein the operation processing unit comprises:

an eighth multiplexer for receiving the values f1, f1/2, and f1/4 from the shift right and providing one of the values under the control of the controller,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value f1 from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, the present luminance signal, and a value from the shift right as a converted luminance signal under the control of the controller.

10. (Cancelled).

11. (Currently Amended) A device as claimed in claim 24~~-28~~, wherein the operand mapping unit comprises:

a third multiplexer for providing one of the present luminance signal and the previous luminance signal as a first initial operand value 'a' to the numerator generating unit, and

a fourth multiplexer for providing one of the present luminance signal and the previous luminance signal as a second initial operand value 'b' to the numerator generating unit.

12. (Previously Presented) A device as claimed in claim 11, wherein the numerator generating unit comprises:

a first shift left for shifting the value >a= from the third multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the value >a=, which are first intermediate operands,

a second shift left for shifting the value >b= from the fourth multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the value >b=, which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining final operands and the numerator portion in the conversion equation from the first intermediate operands and the second intermediate operands.

13. (Previously Presented) A device as claimed in claim 12, wherein the operation processing unit comprises:

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the controller,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the controller,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the controller,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and A0" and selectively providing any one of the received ones under the control of the controller,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

an operator for selectively subjecting a value from the third multiplexer and a value from the fourth multiplexer to a different operation,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator portion f1 of the conversion equation.

14. (Original) A device as claimed in claim 13, wherein the operator is either an adder or a subtracter.

15. (Currently Amended) A device as claimed in claim 24 ~~28~~, wherein the denominator generating unit comprises:

a shift right shifting the numerator portion f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values 2, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator portion of the conversion [operation] equation and a luminance signal having a final converted format using the plurality of values.

16. (Previously Presented) A device as claimed in claim 15, wherein the operation processing unit comprises:

an eighth multiplexer for receiving the values f1, f1/2, and f1/4 from the shift right and providing one of the values under the control of the controller,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value f1 from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, a present chrominance signal, and a value from the shift right as a converted chrominance signal under the control of the controller.

17. (Currently Amended) A digital television receiver, comprising:

an antenna;

a tuner for synchronizing to a desired channel signal;

an intermediate frequency signal generating unit for generating an intermediate frequency signal of the synchronized channel signal;

an audio signal processing unit for processing an audio signal ~~only~~ in the intermediate frequency signal so that the audio signal is audible;

a video signal processing unit for processing a video signal ~~only~~ in the intermediate frequency signal for obtaining chrominance signals and a luminance signal;

a filter unit for low pass filtering the video signal from the video signal processing unit;

a vertical format converting unit for converting a video signal format from the filter unit in a vertical direction to match to a desired output signal format; and,

a horizontal format converting unit for converting a video signal format from the vertical format converting unit in a horizontal direction to match to a desired output video signal format, wherein each of the vertical format converting unit and the horizontal format converting unit includes;

a control unit for determining an operation conducted at the present time, recognizing an operation to be conducted at the next time based on the operation conducted at the present time, and providing control signals suitable for the operation to be conducted at the next time, according to an input video format of an input video signal and an output video format of an output video signal desired to provide,

a first processing unit for converting a luminance signal format in the input video signal into a desired output video format,

a second processing unit for converting a chrominance signal format in the input video signal into a desired output video format, and

a separating unit for separating the received video signal into chrominance signals and a luminance signal.

18. (Original) A device as claimed in claim 17, wherein the first processing unit includes;

a delay for delaying a received luminance signal,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation

from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

19. (Original) A device as claimed in claim 18, wherein the operand mapping unit includes;

a first multiplexer for providing a first value 'a', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently, and

a second multiplexer for providing a second value 'b', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently.

20. (Original) A device as claimed in claim 18, wherein the numerator generating unit includes;

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the first value 'a', which are first intermediate operands,

a second shift left for shifting the second value 'b' from the second multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the second value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining the final operands and the numerators in the conversion operation equation from the first intermediate operands and the second intermediate operands.

21. (Original) A device as claimed in claim 18, wherein the denominator generating unit shifts the numerator f1 from the numerator generating unit by units of (n)th power (n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values ½, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator of the conversion operation equation and a luminance signal having a final converted format using the plurality of values.

22. (Original) A device as claimed in claim 17, wherein the second processing unit includes;

a delay for delaying a chrominance signal,

an averaging unit for averaging a chrominance signal Cn-1 received presently and the chrominance signal delayed in the delay,

a first multiplexer for selectively providing either one of the chrominance signal received presently and a value from the averaging unit under the control of the control unit, and

a second multiplexer for selectively providing either one of the chrominance signal Cn delayed in the delay and a value from the averaging unit under the control of the control unit,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation

from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

23. (Original) A device as claimed in claim 17, further comprising a ratio detecting unit for detecting a format conversion ratio from an input video format to an output video format and providing the detected format conversion ratio to the vertical format converting unit and the horizontal format converting unit.

24. (Currently Amended) A device for converting a video format, comprising:

a controller determining a conversion equation to convert a video signal into a desired format based on a conversion mode, the conversion equation have a numerator portion and a denominator portion, and outputting control signals based on the determined conversion equation;

a numerator generating unit receiving at least one of a present video signal and a previous video signal, configuring to calculate the numerator portion of the conversion equation in response to the control signals, and calculating the numerator portion using the received at least one of present and previous signals; ~~and~~

a denominator generating unit receiving output of the numerator generating unit, configuring to divide the output of the numerator generating unit by the denominator portion in response to the control signals, and dividing the output of the numerator generating unit by the denominator portion to obtain output video signal of the desired format;

an operand mapping unit receiving the present luminance signal and the previous luminance signal, and selectively supplying the present luminance signal and the previous luminance signal to components of the numerator generating unit;

an averaging unit averaging the present chrominance signal and the previous chrominance signal to obtain and averaged chrominance signal;

a first multiplexer selectively outputting one of the averaged chrominance signal and the present chrominance signal;

a second multiplexer selectively outputting one of the averaged chrominance signal and the previous chrominance signal; and

an operand mapping unit receiving output from the first and second multiplexers, and selectively supplying the output from the first and second multiplexers to components of the denominator generating unit.

25. (Previously Presented) The device as claimed in claim 24, wherein the present and previous video signals are luminance signals.

26. (Cancelled)

27. (Previously Presented) The device as claimed in claim 24, wherein the present and previous video signals are chrominance signals.

Claims 28-29. (Cancelled)

30. (Previously Presented) A device for converting a video format, comprising

a control unit determining an operation to convert an input video signal into a video signal of desired format, the determined operation including at least one of a multiplication operation and a division operation; and

a processing unit performing the determined operation based on control signals from the control unit, the processing unit performing the at least one of the multiplication operation and the division operation by shifting in a shifter a value to be one of multiplied and divided.

31. (Cancelled)

32. (New) A device for converting a video format, comprising:

a controller determining a conversion equation to convert a video signal into a desired format based on a conversion mode, the conversion equation have a numerator portion and a denominator portion, and outputting control signals based on the determined conversion equation;

a numerator generating unit receiving at least one of a present video signal and a previous video signal, configuring to calculate the numerator portion of the conversion equation in response to the control signals, and calculating the numerator portion using the received at least one of present and previous signals; and

a denominator generating unit receiving output of the numerator generating unit, configuring to divide the output of the numerator generating unit by the denominator portion in response to the control signals, and dividing the output of the numerator generating unit by the denominator portion to obtain output video signal of the desired format,

wherein the denominator generating unit comprises:

a shift right shifting the numerator portion f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values 2, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator portion of the conversion equation and a luminance signal having a final converted format using the plurality of values.